CURRICULAM VITAE

Dr. K.V.Ramana Rao
Associate Professor

Address:

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Career Objective:

To work in a recognized establishment to fully utilize my professional expertise of teaching and industrial experience and making a significant contribution to the growth of the organization.

Academics:

- Awarded Ph.D (Radar Image Processing) from A.U.C.E in June, 2019.
- Completed M.Tech (Radar & Microwave Engineering) from A.U.C.E with 8.5 CGPA in 2012.
- Completed B.E (Electronics & Communications Engineering) from A.U.C.E with 63% in 1994.
- Completed D.E.C.E (Electronics & Communications Engineering) from Andhra Polytechnic, Kakinada with 72% in 1990.
- Completed SSC from Z.N.V.R High School, Penugonda, W.G.Dt, with 77% in 1986.

Teaching & Industrial Experience:

- Working as an Associate Professor in Dr. Lankapalli Bullayya College of Engineering, Visakhapatnam from 2nd Aug 2023 to till date.
- Worked as an Associate Professor in Sanketika Vidya Parishad Engineering College, Visakhapatnam from 14th February 2022 to 31st July 2023.
- Worked as an Associate Professor in Vignan's Institute of Engineering for Women, Visakhapatnam from 25th January, 2016 to 10th February, 2022.
- Worked as an Associate Professor in Pydah College of Engineering & Technology, Visakhapatnam from 28th June, 2004 to 16th Dec, 2015.
- Worked as an Associate Manager in Bharat Aluminium Co. Ltd for 7 years, 21.01.1997 to 06.02.2004.

Positions Held:

- HOD (ECE) in Sanketika Vidya Parishad Engineering College.
- Head-Placements in Vignan's Institute of Engineering for Women.
- NBA Criteria-6 Coordinator, DSD-DICA Course Coordinator.
- HOD (ECE) in Pydah College of Engineering & Technology.

Technical Expertise:

- Attended SIEMENS Programmable Logic Controllers training conducted at Nashik from 16-11-1999 to 26-11-1999.
- **Simulator software tools:** Xilinx, ENVI 5.0, SNAP.

- ELECTRONIC DEVICES & CIRCUITS
- ELECTRONIC CIRCUIT ANALYSIS
- SWITCHING THEORY & LOGIC DESIGN
- SIGNALS & SYSTEMS
- PULSE AND DIGITAL CIRCUITS
- DIGITAL IC APPLICATIONS
- VLSI
- DIGITAL SIGNAL PROCESSING
- MICROWAVE ENGINEERING
- RADAR SYSTEMS
- DIGITAL SYSTEM DESIGN (M. TECH)
- DESIGN OF FAULT TOLERANT SYSTEMS (M. TECH)

Publications:
International Journals:

1. **K.V.Ramana Rao**, Dr. P. Rajesh Kumar, Assessment of backscattering coefficient measurement of ENVISAT- ASAR data, Journal of Advanced Research in Dynamical and Control Systems, Volume: 9,Issue:16, December, ISSN:1943-023X, [SCOPUS].

2. **K.V.Ramana Rao**, Dr. P. Rajesh Kumar, A Novel Decision Tree Algorithm for Land Cover Classification Using Hybrid Polarimetric SAR Data, International Journal of Research, Volume: 4 Issue:17,e-ISSN: 2348-6848, 2017.

3. **K.V.Ramana Rao**, Dr. P. Rajesh Kumar, Land Cover Classification Using SENTINEL-1 SAR Data, International Journal for Research in Applied Science & Engineering Technology, Volume:5, Issue: XII, ISSN: 2321-9653 2017.

4. **K.V.Ramana Rao**, Dr. P. Rajesh Kumar, Backscattering-coefficient measurement and land use land cover classification using ENVISAT-ASAR data, International Journal of Engineering & Technology(UAE), Volume:7,doi:10.14419/ijet.v7i2.9858, ISSN 2227-524X, 2018, [SCOPUS].

5. **K.V.Ramana Rao**, Dr. P. Rajesh Kumar, Land use land cover classification using unsupervised classifiers and various polarimetric SAR data types, Anveshana's international journal of research in engineering and applied sciences, Volume: 3, Issue: 03, ISSN-2455-6300, 2018.

6. **K.V.Ramana Rao**, Dr. P. Rajesh Kumar, Land cover classification using LANDSAT-8 optical data and Supervised Classifiers, International Journal of Engineering & Technology(UAE), Volume:7, Issue:2 DOI:10.14419/ijet.v7i2.17.11567 ISSN-2227-524X, [SCOPUS].

7. **Dr.K.V.Ramana Rao**, B.S.V.S.N.M. Lalitha Sree, B. Jahanavi Rani , K.V.V.S Harshitha, CH. Preethi, Removal of speckle noise using different filters, Journal of education: Rabindra bharati university, Volume:23 Issue:7,ISSN: 0972-7175, 2021.

8. **Dr.K.V.Ramana Rao**, P. Yasodakrishna, P. Sri Divya, T. Supraja, M. Niharika, Analysis of various speckle filters based on window size and its impact on speckle noise, Journal of Fundamental & Comparative Research, Volume:7 Issue:4, ISSN: 2277-7067, 2021.

9. G. Tulasi, B. Sri Vasavi, B. Bhargavi, K. Priyanka, **Dr. K.V.RAMANA RAO**,

Polsar image classification using context based max-margin, Dogo Rangsang Research Journal, Volume:10 Issue:7,ISSN: 2347-7180, 2020.

10. **Dr.K.V.Ramana Rao**, Dr. Nagendra babu Mahapatruni , Velanginisarat P & Kallempudi Vahini, Implementation strategy to minimize the speckle noise from polarimetric SAR data, International Journal of Mechanical and Production Engineering Research and Development, Volume:10 Issue:3,ISSN(P): 2249–6890; ISSN(E): 2249–8001 , 2020. [SCOPUS]

11. Dr. P Sudhakar, **Dr. K.V.Ramana Rao**, P Gopi Krishna, N J Rama Krishna, Nonlinearity performance analysis of Gaussian weighted adaptive residual unscented particle filter, Solid State Technology, Volume: 63 Issue:5, ISSN: 0038-111X, 2020.[SCOPUS]

12. Dr. Nagendra babu Mahapatruni, **Dr. KV Ramana Rao** , P Velangini Sarat, Munmun Bhaumik, Unmanned ground robot for diffusing explosives with surveillance, Indian Journal of Science and Technology, Volume:13,Issue:31,ISSN Print: 0974-6846 Electronic: 0974-5645, 2020, Impact factor 3.331, [Web of Science].

13. S. SINDHURI1 , **K. V. RAMANA RAO**, Underlaying MIMO System for D2D Communication, International Journal of Advanced Technology and Innovative Research, Volume10,Issue:02, ISSN:2348–2370, 2018.

14. D. Pavana kumari**, K.V.Ramana Rao**, Bhaskara Rao Doddi, Full Custom Design of Low Power 8-bit Magnitude Comparator with Small Transistor Count by Static CMOS, International Journal of Advanced Research in Computer Engineering & Technology, Volume:3 Issue:9,ISSN: 2278 –1323, 2014.

15. K. Prasanna Kumar , **K.V.Ramana Rao** , R. Vijaya Durga, FPGA Implementation of DSWG Using Cordic Algorithm, International Journal of Innovative Research in Computer and Communication Engineering, Volume:1 , Issue:7, ISSN(Online): 2320-9801, 2013.

16. R. Vijaya Durga, **K. V. Ramana Rao**, K. Prasanna Kumar, Implementation of Cryptography Architecture with High Secure Core, International Journal of Modern Engineering Research, IJMER, Volume:3, Issue.4,ISSN: 2249-6645, 2013.

17. M. Bala Bhanu, P.Deepthi, **K.V.Ramana Rao**, Simulation Analysis Of Real-Time Sign7al Processor For Pulse Doppler Radar, International Journal of Scientific & Technology Research, (IJSTR) Volume: 2, Issue:10, ISSN 2277-8616, 2013.

18. S. Ravi Chandra Kishore, **K.V. Ramana Rao** , Implementation of carry-save adders in FPGA, International Journal of Engineering and Advanced Technology (IJEAT), Volume:1, Issue:6, ISSN:2249–8958, 2012, DOI: https://doi.org/10.35940/ijeat.2249-8958.

19. S. Rajeswari, P.Deepthi, **K.V.Ramana Rao** , Image Compression Technique using Two Dimensional Discrete Cosine Transform, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume:1,Issue:4, ISSN:2278-3075,2012

20. P. Surya Chandra, **K.V. Ramana Rao**, Ramesh P, L. N. Chaitanya, Pradeep U.K, Design of Simulated Software for Analysis and Studies of Computer organization, International Journal of Computer Applications, IJCA Volume: 48, Issue: 10, ISSN: 0975–8887, 2012.

21. M. Ashok Chakravarthi, **K.V. Ramana Rao**, A VLSI Implementation of Modulo $(2^n -1)$ Multiplier By Using Radix-8 Modified Booth Algorithm,

International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume: 1, Issue: 5, ISSN: 2278-3075 2012.

22. Glory Priscilla N., P.Deepthi, **K.V.Ramana Rao** , VLSI Implementation of Viterbi decoder in MIMO Systems, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume:1 Issue:5, ISSN: 2278-3075, 2012.

23. Vivekananda M, Dr. R. P. Das, **K.V.Ramana Rao** ,Two Dimensional Cellular Automata for Pseudo Random Number Generation, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume:1, Issue:6 , ISSN: 2278-3075, 2012.

24. Ganesh Kumar B, Dr. R. P. Das, **K.V.Ramana Rao** , Design of High Speed CODEC for On Chip Cross Talk Avoidance, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume:1 , Issue:5,ISSN: 2278-3075, 2012.

25. K. Bala Souri, K. Hima Bindu, **K.V. Ramana Rao**, A Built-In Self-Repair Scheme for Random Access Memories with 2-D Redundancy, International Journal of Soft Computing and Engineering (IJSCE), Volume:1, Issue:5,ISSN:2231-2307, 2011.

26. K. Hima Bindu, K. Bala Souri, **K.V. Ramana Rao**, MAC Architecture– Accumulator Based on Booth Encoding Parallel Multiplier, International Journal of Soft Computing and Engineering (IJSCE), Volume:1 , Issue:5, ISSN: 2231-2307, 2011.

27. Shaik Ayesha, B.V. Ramana, **K.V. Ramana Rao**, Floating-Point FPGA: Architecture Performance and Modeling, International Journal of Soft Computing and Engineering (IJSCE), Volume: 1, Issue: 5, ISSN: 2231-2307, 2011.

28. AP, N. Suresh Kumar, G. Babu Rao, K.V.Ramana Rao, Clock Synchronization in Digital Circuits, International Journal of Engineering Trends and Technology 2 (2), 42-44, 2011.

29. NS Kumar, DVR Reddy, A Patro, KVR Rao Method to Minimize Data Losses in Multi Stage Flip Flop, GJRE (F) 11 (6), 2011.

30. KVR, E. Raja, Implementation of Multilayer AHB Bus matrix for ARM, International Journal of Soft Computing and Engineering (IJSCE) 1 (5), 27-30, 2011.

31. KVRR, B. Rajani Kumari, Dynamic Power Suppression Technique in Booth Multipliers, International Journal of Innovative Technology and Exploring Engineering 1(4), 47-49, 2012.

32. KVRR, Sai Lakshmi Kumari N, U. Pradeep Kumar, Implementation of 2D Hartley transform using Distributed Arithmetic, International Journal of Innovative Technology and Exploring Engineering 1(5), 1-3, 2012.

33. KVRR, Swathi Gera, M. Ashok Kumar, Implementation of Coordinate Rotation algorithm for Hardware Multipliers, International Journal of Innovative Technology and Exploring Engineering, 1(5), 10-12, 2012.

34. KRR, U. Supriya, Design of Low Power CMOS Circuits using Leakage Control Transistor and Multi-Threshold CMOS Techniques, , International Journal of Computer Technology and Applications, 3(4), 1496-1500, 2012.

35. PSS, Dr. K. V. Ramana Rao, Ch. Sandhya Rani, S. Shiva Chaitanya, G. Venkat Removal of Speckle Noise From SAR Images Using Various Filters, INTERNATIONAL JOURNAL OF ENGINEERING RESEARCH & TECHNOLOGY 12 (5), 135-145, 2023.

36. KVRRAO, G. DEEPIKA, Implementation of an Area and Power Optimized Fault Detection Circuit Using Low Transition Method, International Journal of Scientific Engineering and Technology Research 3(39), 7905-7909, 2014.
37. KVRR, K. Madhavi, Particle Swarm Optimization Approach for MST Problem in VLSI Routing, CiiT International Journal Programmable Device Circuits and Systems 5, 2013.

Conference Proceedings:

K.V.Ramana Rao, Dr. P. Rajesh Kumar, Land use land cover classification using a novel decision tree algorithm and Satellite Data Sets, International conference on information system design and intelligent applications, Volume:1, ISSN-2194-5357, 2019,], doi.org/10.1007/978-981-13-3329-3_35. [SPRINGER]

Workshops Attended:

- "Telecommunication and Information Technology" conducted by FALCON ELECTRO-TEK PVT. LTD. In Visakhapatnam on 10th December 2007.
- "Environmental Awareness Campaign" one day seminar sponsored by A.P. Pollution Control Board, Visakhapatnam organized on 16th March 2011.
- "MATLAB & Its Applications in Communications and Signal processing" conducted by E.C.E department of A.U.C.E on 12th & 13th Nov, 2011.
- "Latest Technologies in Electronic Communications" organized by E.C.E department of MVGR college of engineering on 22nd& 23rd Dec, 2011.
- "Outcome Based Engineering Education" conducted by JNTUK on 5th Feb, 2013.
- "Advances in Signal Processing" organized by E.C.E department of A.U.C.E on 30th&   31st Aug, 2013.
- "Integrated Systems Health Management" (WISHM) organized by Vignan's Institute of Engineering for Women from 27th and 28th May, 2016.
- "Mixed Signal To Design Using Graphics EDA Tools (WMSID16")" organized by Vignan's Institute of Engineering for Women from 14th and 15th June, 2016.
- "Engineering Education & Research" conducted by National Instruments India on 7th September 2016.
- Geospatial World Forum 2017 organized by Geospatial media + communications in Hyderabad from 22nd to 25th January 2017.
- "Build a Bot" Workshop organized as a part of RPA Explorer Day at GVP College of Engineering (Autonomous) in association with UiPath held on 15th November 2019.
- A Two Day Multidisciplinary International Conference on emerging trends and technologies in Engineering, Pharmacy and Langlit conducted on 29th & 30th April 2022 in Sanketika Vidya Parishad Engineering College.

Faculty Development Programs:

- "NBA ACCREDITATION PROCEDURES" conducted in Vignan's Institute of Engineering for Women, Visakhapatnam November 2018.
- "CMOS Integrated Circuits for Instrumentation and IOT Applications", conducted in Vignan's Institute of Engineering for Women, Visakhapatnam, from 29th October to 3rd November 2019.

- "Entrepreneurship Development" sponsored by Department of Science and Technology, Govt. of India, organized by National Institute for Micro, Small and Medium enterprises (ni-msme) in Vignan's Institute of Information & Technology, Visakhapatnam from 10th February to 22nd February 2020.

Achievements:
- Got school second rank in IX Class (1985) & X Class (1986), Z.N.V.R. High school, Penugonda, W.G.Dt.
- Qualified in I.E.S written examination conducted in 1996.
- Got 57th rank in PGECET, conducted in 2010.
- Got 28th rank in AURCET-2013.

Events Organized:
- Convener for National Level Technical Symposia INVENTO-2K9 conducted in 2009.
- Convener for National Level Technical Symposia INVENTO-2K12 conducted in 2012.
- Convener for National Level Technical Symposia PEARL-FETE conducted in 2014.
- Zonal coordinator for Robotryst-2015 workshop conducted in association with IIT, Delhi.

Projects Guided:
- **B. Tech: 24**
- **M.Tech: 17**

Extra Curricular Activities:
- Coordinator for Environmental Awareness Campaign conducted in Pydah College of engineering & Technology, 2011.
- Transport Coordinator for Vignan's Institute of Engineering for Women to participate in VIZAG NAVY MARATHON, 2018.
- Transport Coordinator for Vignan's Institute of Engineering for Women to participate in YUVATARANG 2K19 conducted in VIIT, Visakhapatnam.
- Events Coordinator for SANKETH-2K23, Annual Day of Sanketika Vidya Parishad Engineering College.

Personal Information:
Date of Birth	: 12-08-1971
Father's name	: K. Satyanarayana
Languages Known	: Telugu, English & Hindi
Permanent Address	: F. No: S/2, G. R. Towers, Railway New Colony, VSP-16

(Dr. K.V. RAMANA RAO)